REMARKS

This paper is filed in response to the office action mailed on January 4, 2005.

Claims 1-6 stand rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite. In response, claims 1, 3, 4 and 6 have been amended to traverse this rejection. Further, the spacers 22a, 22b of Fig. 1f have also been appropriately labeled in the new drawings submitted herewith. Formal drawings for Figs. 1e-1f are attached hereto as an appendix.

Applicant respectfully submit that claims 1 and 4 are in full compliance with 35 U.S.C. § 112, second paragraph as each claim element is clearly described in the drawings.

Specifically, claim 1 is directed toward a method for fabricating a merged logic device that comprises forming a high voltage p-type well region 12 and a logic region 30 on a semiconductor substrate 11 as shown in Fig. 1a. Claim 1 then recites the conducting of an ion implantation for forming a logic p-type well region 14 on the logic region 30 and a high voltage n-type well region 15 on the high voltage p-type well region 12 as shown in Fig. 1b. Claim 1 then recites forming a high voltage gate oxide film 16a on the resulting structure and conducting a threshold voltage ion implantation process as shown in Fig. 1c. Then, as shown in Fig. 1d, claim 1 recites forming a logic gate oxide film 16b on the logic region 30 and forming a logic gate electrode 17a on the logic region and a high voltage gate electrode 17b on the high voltage p-type well region 12. Then, as shown in Fig. 1e, claim 1 recites forming a logic double diffused drain region 18 on the logic region and forming spacers 22a, 22b on the electrodes 17a and 17b, respectively. Then, as shown in Fig. 1f, claim 1 recites forming logic source/drain regions 19 and high voltage source/drain regions 20 as well as a bulk bias region 21.

Claim 4 then recites the forming of a high voltage p-type well region 12 and a logic region 30 on a semiconductor substrate as shown in Fig. 1a. Claim 4 then recites conducting an ion implantation for forming a p-type well region 14 on the logic region 30 and a high voltage n-type well region 15 on the high voltage p-type well region 12 as shown in Fig. 1b. Claim 4 then recites forming a high voltage gate oxide film 16a on the resulting structure and conducting a threshold voltage ion implantation process as shown in Fig. 1c. Claim 4 then cites forming a logic gate oxide film 16b on the logic region 30 as shown in Fig. 1d. Claim 4 then recites forming a logic gate electrode 17a on the logic region 30 and the

high voltage gate electrode 17b on the high voltage p-type well region 12 as shown in Fig. 1d. Then, as shown in Fig. 1e, claim 4 recites forming a logic DDD region 18. Finally, as shown in Fig. 1f, claim 4 recites forming the spacers 22a, 22b, the logic source/drain region 19, the high voltage source/drain region 20 and the bulk region bias region 21 as shown in Fig. 1f.

Applicant respectfully submits that in view of the amendments to claims 1, 3, 4 and 6, all indefiniteness rejections have been traversed.

As the prior art does not teach or suggest the methods of independent claims 1 and 4, applicant respectfully submits that claims 1-6 are in a condition for allowance and an early action so indicating is respectfully requested.

The Commissioner is authorized to charge any fee deficiency required by this paper, or credit any overpayment, to Deposit Account No. 13-2855.

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Respectfully submitted,

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